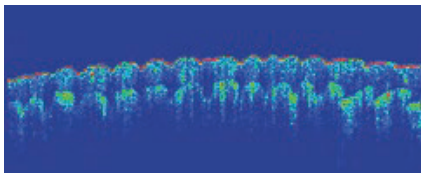
YELLOWSYS

High-Resolution Optical Coherence Tomography Core

Overview

Swept-Source Optical Coherence Tomography (SS-OCT) allows for non-invasive, high-speed, high-resolution imaging in various biomedical or industrial applications. Particularly with optical swept sources in the longer wavelength range (e.g., 1310 nm) new imaging capabilities exist that have not been addressable with time-domain or camera-based OCT systems.

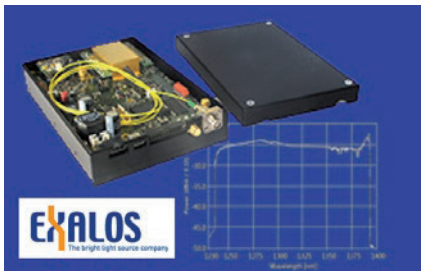


B-SCAN OF HUMAN SKIN

SS-OCT systems require, besides a swept source and a balanced optical receiver, fast and high-resolution data acquisition (DAQ) cards that capture the raw OCT signal. The so-called k-clock reference signal is used for the data acquisition in two possible ways:

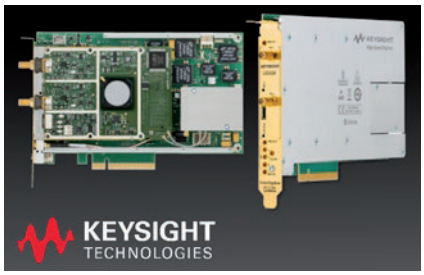
1. As an external clock for the ADC that captures the OCT signal at times of equidistant frequency positions.

2. Acquired in parallel to the OCT signal on a second ADC with both ADCs being clocked internally at a fixed and constant frequency.



EXALOS' SWEPT-SOURCE

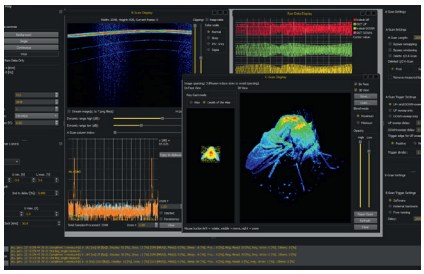
The second approach is generally more robust in terms of data acquisition and is suitable to handle a greater variety of linear and nonlinear swept sources. But, it requires a fair amount of signal processing that can be accomplished in real time with a deterministic latency and reliable throughput using a DAQ card with an on-board FPGA.



KEYSIGHT DIGITIZER WITH FPGA

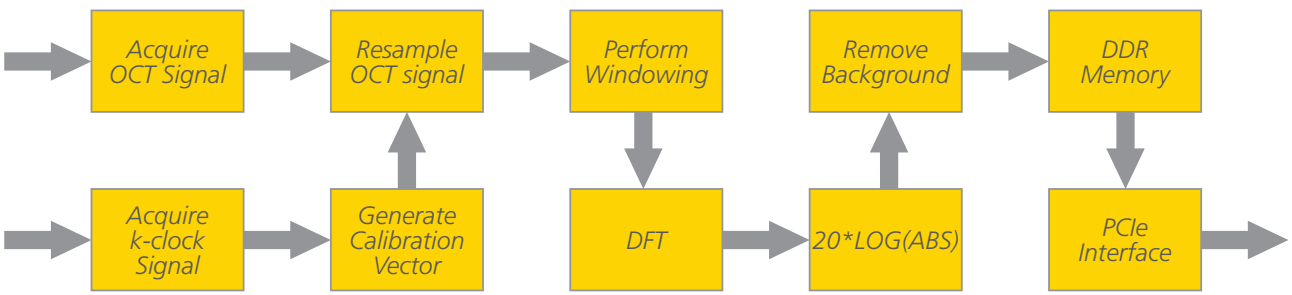
Product description

The OCT-Core receives the OCT signal and the k-clock reference signal from two ADCs along with an A-scan and B-scan trigger. For each A-scan, a remapping vector is generated from the k-clock using a Hilbert transform. This remapping vector is then used to resample the OCT signal that is equidistant in the frequency domain (k-space) before the FFT can be applied. Real-time background subtraction and dispersion compensation can be enabled. The FFT output (20·log) is stored in on-board DDR memory before being streamed to the host PC through a PCI-Express interface. Raw data are available for debug purposes. Users can control the system and readout the data through hardware registers or from the provided API. A complete demo/startup system (OCT-Engine) is available as an option. YellowSys' OCT-Core is based on a VHDL code, packaged as a blackbox with well-defined interfaces, and has been integrated for Keysight digitizers (currently type U5303A).



YELLOWSYS GRAPHICAL USER INTERFACE (GUI)

OCT-Core Bloc Schematic



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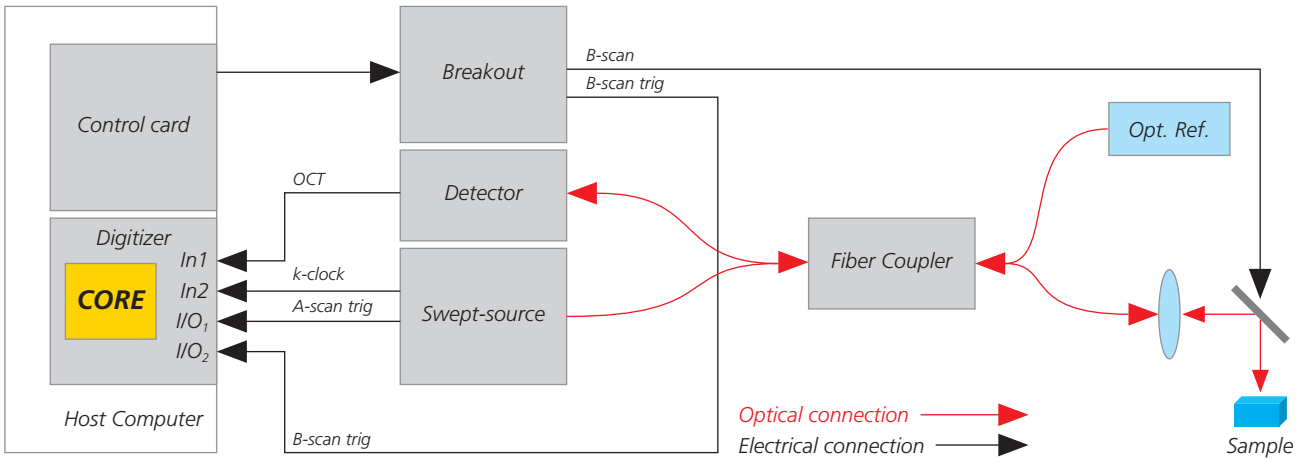
Example System



Specifications : OCT

A-scan rate	10 to 100 kHz or 200 kHz (hardware option)
A-scan length	2048 FFT points, mirrored
Imaging range	8-10 mm in air (OCT-Engine)
OCT sensitivities	>100 dB with 1.5 mW in the sample arm (OCT-Engine)
A-scan averaging	Up to 128-times averaging in real time
B-scan width	Adjustable, 4-2048 A-scans/B-scan (OCT-Engine)
B-scan rate	20 fps
Additional features	Phase Sensitive, Dispersion Compensation, Continuous Acquisitions Mode

Specifications: Acquisition / FPGA

FPGA Xilinx	Virtex-6 LX195 (minimum)
ADC	12-bit @ 500 MS/s or 1 GS/s (hardware option)
Full-Scale Range (FSR)	1 Vpp or 2 Vpp selectable (U5303A)
Coupling	50 Ohms, DC coupled (U5303A)
System (min.):	Windows 7, 8 GB RAM, i7, 1 slot: PCIe Gen2 x4, 2 x 5.25" HDD drive bay

Ordering / Options

OCT-CORE	OCT-CORE: FPGA Core with real-time SS-OCT processing block that converts OCT data and k-clock signals (input) to high performance Ascans (output). Includes: C++ and LabView API for an efficient software integration, complete 2D GUI. Order to www.magentasys.com
OCT-3D	3D visualization option for the GUI. Order to www.magentasys.com
OCT-ENGINE	Turnkey solution based on the OCT-Core, including host PC, built-in OEM swept source with integrated k-clock, fast data acquisition with on-board FPGA, low-speed control card (for scanner control, optional), optical balanced receiver (optional) and software GUI. For more info, please contact: www.exalos.com